	FILE 'JPO' E	ENT	TERED AT 13:16:01 ON 11 APR 1999
L15	48	s	L1
L16	794	S	L2
L17	44	S	L3
L18	621	S	L4
L19	0	S	L1 AND L2 AND L3 AND L4
L20	0	S	L1 AND L2
L21	0	S	L2 AND L3
L22	0	S	L4 AND L2
L23	0	S	L4 AND L1
L24	5	S	LATCH### (W) DATA (W) SIGNAL
L25	3540	S	DELAY (2W) SIGNAL
L26	334	S	(GENERAT###(5A)DATA)(2P)((DATA)(4A)(COMPARATOR))
L27	0	S	L26 AND L24
L28	0	S	L24 AND L25 AND L26
L29	1	S	L25 AND L26
L30	0	s	L15 AND L16
L31	0	s	L17 AND L15
L32	0	S	L16 AND L17

.

1. 5,777,624, Jul. 7, 1998, Method and apparatus for eliminating visual artifacts caused by diffusing errors in a decimated video signal; Bill A. Munson, 345/431 [IMAGE AVAILABLE]

=> d 110 kwic, ab

US PAT NO: 5,777,624 [IMAGE AVAILABLE] L10: 1 of 1

DETDESC:

DETD(137)

FIG. . . . hardware is updated if there is any change to the occlusion of a video image, i.e., video window. As video data enters the video capture hardware, its destination coordinates are compared with the regions to be clipped. If there is a match, then the data.

CLAIMS:

CLMS(2)

pixel are not the same;

- a second latch for storing a green color component of a pixel in said video signal;
- a **second comparator** receiving said green color component of a pixel in said decimated video signal from said second latch and a green color component of a next pixel in said decimated video signal, said **second comparator** asserting a second signal when said green color component of said pixel and said next pixel are not the same:
- a third latch for storing a blue color component of a pixel in said decimated video signal;
- a third comparator receiving said blue color component of a pixel in said decimated video signal from said **third latch** and a blue color component of a next pixel in said video signal, said third comparator asserting a third signal. . .

ABSTRACT:

Method and apparatus for preventing visual artifacts when converting a 24 bits per pixel red-green-blue (RGB) video signal to a 16 bit per pixel video signal, including a decimator circuit for discarding the least significant bits (LSBs) of the red, green and blue color components of a pixel in the RGB video signal. Further included is an error diffusion circuit coupled to the decimator circuit for adding the LSBs of each of the aforementioned color components of a pixel in the RGB video signal to the LSBs of the same color components of a previous pixel in the RGB video signal and factoring a carry generated by the addition into the MSBs of the same color components of a next pixel in the RGB video signal. An edge detector circuit is coupled to the error diffusion circuit for resetting the error diffusion circuit when the MSBs of the color components of the pixel in the RGB video signal are not the same as the MSBs of the color components of the previous pixel in the RGB video stream.

reach the zero crossing point, therefore, even after has been inputted to a comparator, a tata (g) can be detected normally.

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=> d his

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(FILE 'USPAT' ENTERED AT 13:00:42 ON 11 APR 1999)
L1
          1215 S THIRD (2W) LATCH
          10905 S SECOND (2W) COMPARATOR
L2
L3
          2652 S DATA (3A) CAPTURE
          1933 S ADJUST###(W)SIGNAL
L4
           47 S 713/503/CCLS
L5
L6
          1271 S 375/33#/CCLS
           0 S L6 AND L5
L7
L8
          1318 S L6 OR L5
L9
             0 S L1 AND L2 AND L3 AND L4
             1 S L1 AND L2 AND L3
L10
            14 S L4 AND L3
L11
L12
             0 S L11 AND L1
             0 S L11 AND L2
L13
L14
             0 S L11 AND L8
    FILE 'JPO' ENTERED AT 13:16:01 ON 11 APR 1999
            48 S L1
L15
           794 S L2
L16
            44 S L3
L17
            621 S L4
L18
             0 S L1 AND L2 AND L3 AND L4
L19
             0 S L1 AND L2
L20
             0 S L2 AND L3
L21
L22
             0 S L4 AND L2
             0 S L4 AND L1
L23
            5 S LATCH###(W)DATA(W)SIGNAL
L24
          3540 S DELAY (2W) SIGNAL
L25
          334 S (GENERAT###(5A)DATA)(2P)((DATA)(4A)(COMPARATOR))
L26
L27
             0 S L26 AND L24
L28
             0 S L24 AND L25 AND L26
L29
             1 S L25 AND L26
```

1. JP362175911A , Aug. 1, 1987, STORAGE INFORMATION REPRODUCING CIRCUIT; OKUBO, TOSHIKI, INT-CL: G11B5/09

=> d 129 ab, kwic

JP362175911A

L29: 1 of 1

ABSTRACT:

PURPOSE: To obtain a recording information reproducing circuit for generating no data error caused by noise, by providing an adjusting means for generating a delay signal which has given a prescribed delay to an output of an amplifying/ filter means, executing an addition of this delay signal and that which gives no delay, and outputting its result to a differential means.

CONSTITUTION: A reproducing signal (a) which has been read from a magnetic head is amplified by an amplifier 1, and thereafter, a regular noise is eliminated through a filter 2, and said signal becomes a filter signal (b). A delaying circuit 3 delays the filter signal (b) by a prescribed time T<SB>d</SB>, and thereafter, inputs it as a delay signal (c) to an adder circuit 4. The adder circuit 4 adds the filter signal (b) and the delay signal (c), but the large noise which exists in the filter signal (b) becomes the noise whose phase is opposite to that of the delay signal (c), and after adding them, the unevenness becomes pretty small. Accordingly, in a differential signal (e), the noise which is lowered to a zero crossing point by only the filter signal (b) becomes uneven a little by adding the delay signal (c), and does not reach the zero crossing point, therefore, even after it has been inputted to a comparator, a data (g) can be detected normally.

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ABSTRACT:

PURPOSE: To obtain a recording information reproducing circuit for generating no data error caused by noise, by providing an adjusting means for generating a delay signal which has given a prescribed delay to an output of an amplifying/ filter means, executing an addition of this delay signal and that which gives no delay, and outputting its result to a differential means.

CONSTITUTION: A reproducing signal (a). . . A delaying circuit 3 delays the filter signal (b) by a prescribed time T<SB>d</SB>, and thereafter, inputs it as a **delay signal** (c) to an adder circuit 4. The adder circuit 4 adds the filter signal (b) and the **delay signal** (c), but the large noise which exists in the filter signal (b) becomes the noise whose phase is opposite to that of the **delay signal** (c), and after adding them, the unevenness becomes pretty small. Accordingly, in a differential signal (e), the noise which is lowered to a zero crossing point by only the filter signal (b) becomes uneven a little by adding the **delay signal** (c), and does not